ELECTRO-OPTIC DEVICES, INC.

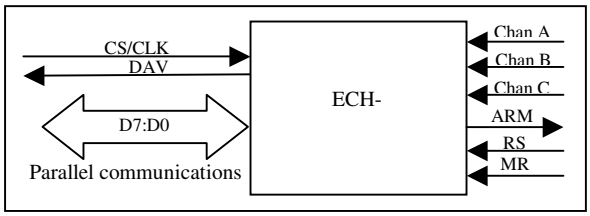
ECH-5A

Fully Asynchronous Single Start Dual Stop Chronometer Module w/ Adjustable Range Gate

(firmware version 1.08)

FEATURES:

- Measurement error < 50ps RMS.
- Range gate adjustable from 1.28 to 261.12 microseconds (selectable in 1.28 µS increments).
- Measurement rate in excess of 25kHz (rates will decrease with longer range gates).
- Simultaneously makes two STOP signal edge measurements using the same START signal edge.
- Can be used as read only or reconfigured through commands.
- Control information and data transfer via synchronous parallel interface.
- Programmable input source and edge selection via configuration command.
- Dual measurements with each ns result sent in 3-byte, 18:6 format. (18-bits whole : 6-bits fractional).
- Optional SMA, SMB or SMC coaxial connections for timing signals.
- Single 5-Volt supply requirement.



DESCRIPTION:

The ECH-5A is a fully asynchronous dual channel chronometer module. The ECH-5A will accept a single START edge and two STOP edges from signals simultaneously and are programmable for different inputs and edges. The ECH-5A will take samples within a time interval range gate from 1.28µs to 261.12µs at a rate of 25kHz with an accuracy of 50ps RMS. Routine Calibration may be performed periodically using the CALIB signal to keep measurements accurate over the operating temperature range.

Control commands and data transfer are accomplished via synchronous parallel interface. The ECH-5A measures two time intervals for every timing event. Varying combinations of input and edge selection through commands offers more configuration flexibility. Programmable adjustable range gate allow the user to configure the ECH-5A for predictable near or far measurements to help keep repetition rate optimized. The DAV signal informs the host that measurement results are ready to transfer. The two START-to-STOP measurement results are clocked out using the $\overline{CS}$ signal in a three-byte, 18 whole number bits and 6 fractional bits, format in the unit of nanoseconds.

The ECH-5A operates with a single 5Vdc supply typically at 250mA. The ECH-5A is a compact circuit board design available with optional SMA, SMB, or SMC coaxial connections.

INTERFACE:

Connector P1

Pin	Signal	Dir.	Description
1	VCC	-	+5V power supply requirement
2	GND	-	Ground
3	DB7	I/O	Bit-7 (msb) of the data bus.
4	DB6	I/O	Bit-6 of the data bus.
5	DB5	I/O	Bit-5 of the data bus.
6	DB4	I/O	Bit-4 of the data bus.
7	DB3	I/O	Bit-3 of the data bus.
8	DB2	I/O	Bit-2 of the data bus.
9	DB1	I/O	Bit-1 of the data bus.
10	DB0	I/O	Bit-0 (lsb) of the data bus.
11	VCC	-	+5V power supply requirement
12	GND	-	Ground
13	$\overline{MR}$	I	Resets the ECH-5A microprocessor.
14	$\overline{RS}$	I	Resets all counters and timers and puts ECH-5A into ignore mode.
15	RSRV	I	Reserved Input.
16	ARM	O	Lets host know that ECH-5A is armed and ready to take measurements.
17	CLK /$\overline{CS}$	I	Clocks data in and out. Chip Select (CS) when sending commands
18	DAV	O	Signals Data Available.
19	CAL	I	Puts ECH-5A into Calibration mode.
20	NC	-	No Connect.

Coaxial Connectors:

PC-mount SMA, SMB or SMC connector jacks for Channel inputs. These inputs are AC terminated into 50Ω (1/10W) DC terminated into 2.7KΩ (1/10W) (other termination configurations are optional).

J1: Channel A input
J2: Channel B input
J3: Channel C input

Interface Description:
(I = input, O = output, I/O = bidirectional)

DB7:DBO (I/O) – Parallel data bus to send commands to and receive result data from the chronometer. Timing details can be found in the **communication** section.

$\overline{MR}$ (I) - Master Reset input (hardware reset). Logic LOW applied to this input performs a hardware reset on the ECH-5A's main microprocessor.

$\overline{RS}$ (I) – Reset input (counter reset). Logic LOW applied to this input resets all counters and timers and puts the ECH-5A into an ignore mode, which ignores any inputs from the host and ignores any measurement signals.

R/$\overline{W}$ (I) – Read/Write. This signal is not currently used.

ARM (O) – ECH-5A ARM output. When HIGH, informs the host that the ECH-5A is armed, ready and waiting for a measurement. The on-board ARM LED also lights when armed.

CLK/$\overline{CS}$ (I) - Chronometer Chip Select handshake signal. Used during transfer of commands and data between the chronometer module and the host microprocessor. More information and timing details can be found in the **communication** section.

DAV (O) – Data AVailable output flag to the host. This output goes logic HIGH to indicate that measurement information is available and ready to be read by the host system. This output is often used to generate a hardware interrupt at the host. Timing details can be found in the **communication** section.

CAL (I) – CALIBration input. This active high signal puts the ECH-5A into calibration mode. For greater measurement accuracy in extreme conditions, a calibration should be performed frequently. *Note*: Calibration must be performed at least once after $\overline{MR}$ reset or power-up.

OPERATIONAL DESCRIPTION:

Commands:

ID = 0, INPUT SELECT AND POLARITY

byte 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	E2	C2	E1	C1	SE	SC

byte 2
8-bit range-gate increments of 1.28µS.

Where:

BYTE 1
SC: START source channel *(default = 0)*

0 = Channel A input
1 = Channel B input

C1, C2: STOP1 and STOP2 source channel*(default = 0)*

0 = Channel B input
1 = Channel C input

SE, E1, E2: START, STOP1 and STOP2 edge
(default = 1,1,0)

0 = Falling edge
1 = Rising edge

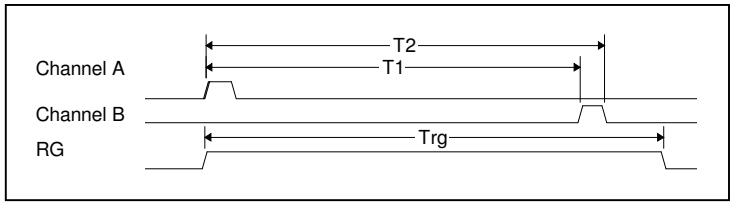
BYTE 2

Range gate value in 1.28µS increments from 1.28µS to 261.12µS. Used to increase range gate for far distant measurements. Default = hex value 0x01 (1.28µS).
Examples:

Default configuration is to simultaneously measure the time interval from the leading-edge of a positive going Channel A pulse (START) to the leading-edge of a positive going Channel B pulse (STOP1) for the first (T1) measurement and the trailing-edge of the same Channel B pulse (STOP2) for a second (T2) measurement. The time between the start and each stop edges must occur within the default configured range gate of 1.28µs. The configuration bits are set as follows:

SC = 0, SE = 1, C1 = 0, E1 = 1, C2 = 0, E2 = 0
RG = 0x01 1.28µs

Diagram 1: This is the default configuration of the ECH-5A after power-up or master reset.



T1 = t_A (rising-edge) to t_B (rising-edge)
T2 = t_A (rising-edge) to t_B (falling-edge)
Trg = t_{START} (rising-edge) to range gate amount.

Alternate configurations are possible to address other timing needs. For instance, pulse width of up to 2.56µs can be measured on a single input when connected to Channel B and the configuration bits are set as follows:

SC = 1, SE = 1, C1 = 0, E1 = 0, C2 = 0, E2 = 0
RG = 0x02 = 2.56µs*
* Repetition rate will decrease with longer measurements.

T1 = T2 = t_B (rising-edge) to t_B (falling-edge)

The two results should be identical with a small amount of offset due to propagation delay differences. This difference should stay consistently constant with each measurement.

Operation:

The following timing diagrams show timing information needed for resetting, sending commands, and calibrating the ECH-5A. As an asynchronous device, the current state of the ECH-5A (measuring or ready to communicate) may be difficult to determine. In order to assure communication is made successfully, the following recommendations should be followed.

First, the Tarm-dav (Diagram 2) shows the maximum time it will take for a measurement to complete from the time ARM goes LOW, to inform the host that a measurement is in progress, to the time DAV goes high, to inform the host of measurement results being available. Before ARM becomes LOW, the ECH-5A will except any of the three RS, $\overline{CS}$, or CALIB signals and execute there functions as required. If ARM become LOW due to a measurement, the ECH-5A will ignore all of these signals until DAV goes HIGH. The result data can then be clocked out of the ECH-5A or the RS signal can be used to discard all result data and enter a reset mode.

Reset mode holds the ECH-5A in a reset or ignore mode. In this mode, the ECH-5A ignores channel inputs (ARM LOW), sending commands, and calibration attempts as well as keeping all counters reset. If a command is to be sent or if a calibration is required, it is recommended to set these signals into their active state while in reset. The reason for this is because $\overline{CS}$ and then the CALIB signals are checked in sequence by the ECH-5A immediately after leaving the reset mode and before ARM returns high to allow the ECH-5A to start a measurement cycle. Activating the $\overline{CS}$ and CALIB signals before RS is released prevents the ECH-5A from starting a measurement cycle before $\overline{CS}$ and CALIB are checked.

Follow these required guidelines for sending commands and calibrating:

1. CLEAR RS signal and wait Trs (Diagram 3).
2. CLEAR $\overline{CS}$ and insert the command data onto the data bus if sending a command to the ECH-5A and/or SET the CALIB signal if calibrating.
3. Set the RS signal to bring the ECH-5A out of reset.
4. a. If sending a command only, wait Trs-cs before setting $\overline{CS}$ HIGH** to clock in the data.
   b. If calibrating only, wait Trs-calib before clearing the CALIB signal.
   c. If sending a command and calibrating, wait Trs-cs before setting $\overline{CS}$ HIGH** and then wait Tcs-calib before clearing the CALIB signal.
5. Once all signals are returned to their inactive state, ARM will return HIGH to indicate that the ECH-5A is ready to receive a new measurement.

** If sending 2-byte commands, clear $\overline{CS}$ and put new data onto the bus then set $\overline{CS}$ again using timing requirements Tcs.

After $\overline{CS}$ and/or CALIB are detected by the ECH-5A, all measurements are ignored and ARM is set to its inactive state. The ECH-5A will not exit the receive command and/or Calibration mode and rearm itself until $\overline{CS}$ and/or CALIB are returned to their inactive states. The ECH-5A uses new command and calibration data until power has been cycled, MR is used for hardware reset, or another command or calibration has been executed to replace it.

Diagram 2: Measurement Timing.

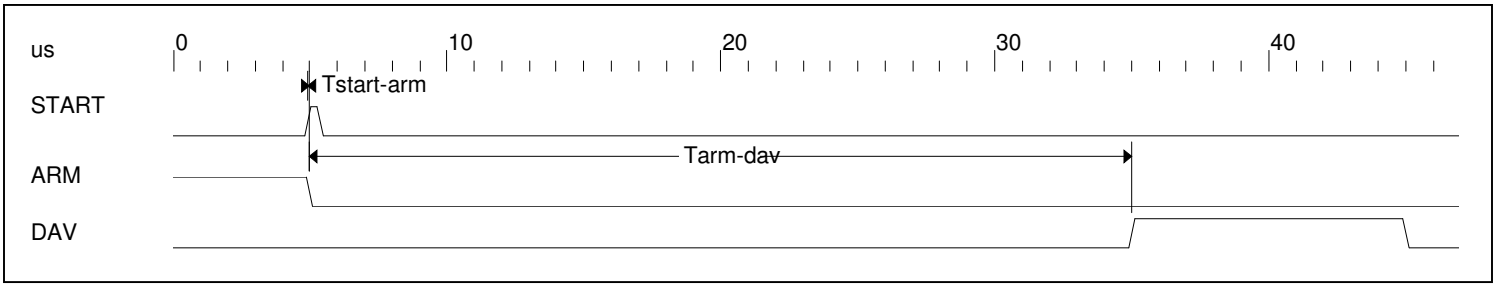


Table 1: Timing under normal operating temperature (25 degrees C).

Event	Description	Time	Unit
Tstart-arm	Time it take ARM to become LOW after receiving a START edge	150	ns
Tarm-dav	Maximum time to take a measurement. **Note 1**	30+RG	µs

Note: Timing is subject to change in future revisions.

1. RG = Range Gate or START-to-STOP time. For every extra µs the measured signal is, it takes an extra µs to capture timing data. It takes less than 30µs to calculate the result after timing data is captured.

Diagram 3: Resetting when ARM is HIGH.

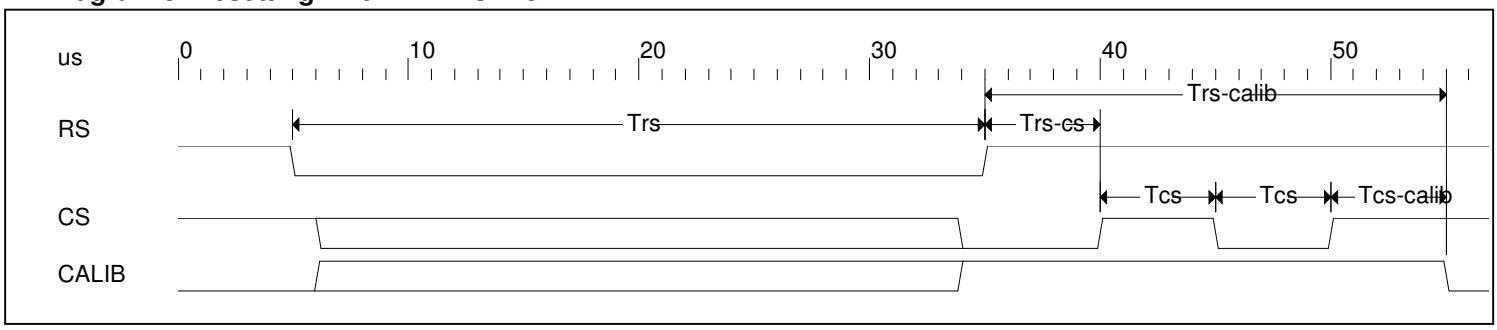


Table 1: Timing under normal operating temperature (25 degrees C).

Event	Description	Time	Unit
Trs	Maximum time RS should have to stay LOW for guaranteed reset.	30	µs
Trs-cs	Maximum time $\overline{CS}$ will need to be held LOW after RS goes HIGH. **Note 1**	5	µs
Tcs	Time $\overline{CS}$ needs to stay HIGH or LOW while clocking in multi-byte commands.	5	µs
Trs-calib	Maximum time CALIB will need to be held HIGH after RS goes HIGH. **Note 2**	5	µs
Tcs-calib	Maximum time CALIB will need to be held HIGH after $\overline{CS}$ goes HIGH. **Note 3**	5	µs
Tcal	Maximum time to Calibrate ECH-5A.	200	µs

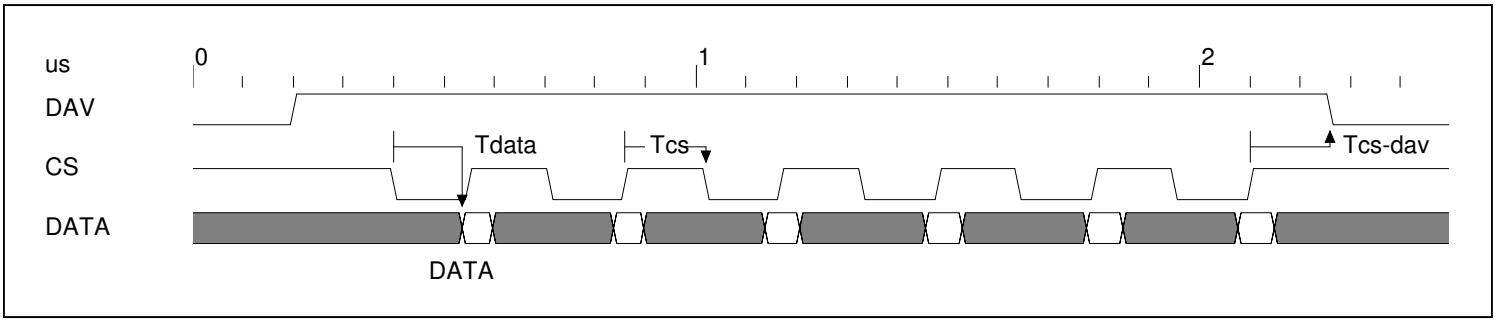
Note: Timing is subject to change in future revisions.

1. Timing values may increase in the future with the amount of usable commands the ECH-5A is capable of receiving and the length of time required to execute commands sent.
2. Time is only relevant when no commands are being sent ($\overline{CS}$ never goes LOW).
3. If sending a 1-byte command, this is the value after the $\overline{CS}$ returns HIGH. If sending a 2-byte (or more) command, this is the time after the last byte is clocked in (the last $\overline{CS}$ should need to return HIGH).

Receiving Results:

The following timing diagram shows the timing requirements for receiving data results from the ECH-5A. The DAV signals to the host that a measurement has been made and results are ready to be transmitted to the host. The host brings $\overline{CS}$ LOW and waits for Tdata time to expire before reading the data byte from the bus. The host can then bring $\overline{CS}$ HIGH for the Tcs required time. All data is clocked in the same way until all four result-bytes are received. After the last data byte is received and $\overline{CS}$ returns HIGH, DAV will return LOW after Tcs-dav time. *Note*: While DAV is HIGH and $\overline{CS}$ is LOW is the only time the data bus is ever set as an output. As soon as $\overline{CS}$ returns HIGH while DAV is HIGH, the data bus returns as an input.

Diagram 4: Clocking in data on the synchronous parallel port.



Event	Description	Time	Unit
Tdata	Maximum time before data is available after $\overline{CS}$ goes LOW.	150	ns
Tcs	Minimum $\overline{CS}$ HIGH time.	160	ns
Tcs-dav	Maximum time before DAV to return LOW after final data byte is clocked.	160	ns

Note: Timing is subject to change in future revisions.

Result Data Format:

Following a ranging event, the two 3-byte (six bytes altogether) results must be read from the ECH-5A (unless $\overline{RS}$ is LOW to discard data). If the measurement was successful, each three-byte data will contain the time interval measurement result, otherwise it will be 0x000000 hex, indicating a failed measurement or no STOP edge was detected after the START edge within the required measurement range gate.

Byte transfer order: (6 bytes total)

These bytes represent the result format from the START edge of the selected START input to the STOP edge of the selected STOP input:

T1 = START to STOP1
T2 = START to STOP2

1st byte = Most Significant Byte of T1.
2nd byte = Center Significant Byte of T1.
3rd byte = Least Significant Byte of T1.
4th byte = Most Significant Byte of T2.
5th byte = Center Significant Byte of T2.
6th byte = Least Significant Byte of T2.

A successful result contains the following data format:

Result Data Bytes (3-byte format)

[18-bit whole number] . [6-bit fractional number]

unit: nanoseconds

The first byte, second byte and the two most significant bits in the third byte contain the whole nanoseconds. The 6 least significant bits in the third byte contains the fractional nanoseconds. In binary format, each three-byte result takes the form:

Byte 1: 2^{17} 2^{16} 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10}
Byte 2: 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2}
Byte 3: 2^{1} 2^{0} **.** 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6}

A failed measurement is generally caused by:

a) Time intervals exceeding range gate.
b) A START signal edge without a STOP signal edge is considered a no-return or out-of-range return pulse.
c) A STOP signal edge received before START edge.
d) Host communication, calibration or auto-rearming coincide with a timing event.

A data result of ZERO (0x000000 hex) will be returned by the ECH-5A for failures a – c above.

ECH-5A ORDERING OPTIONS:

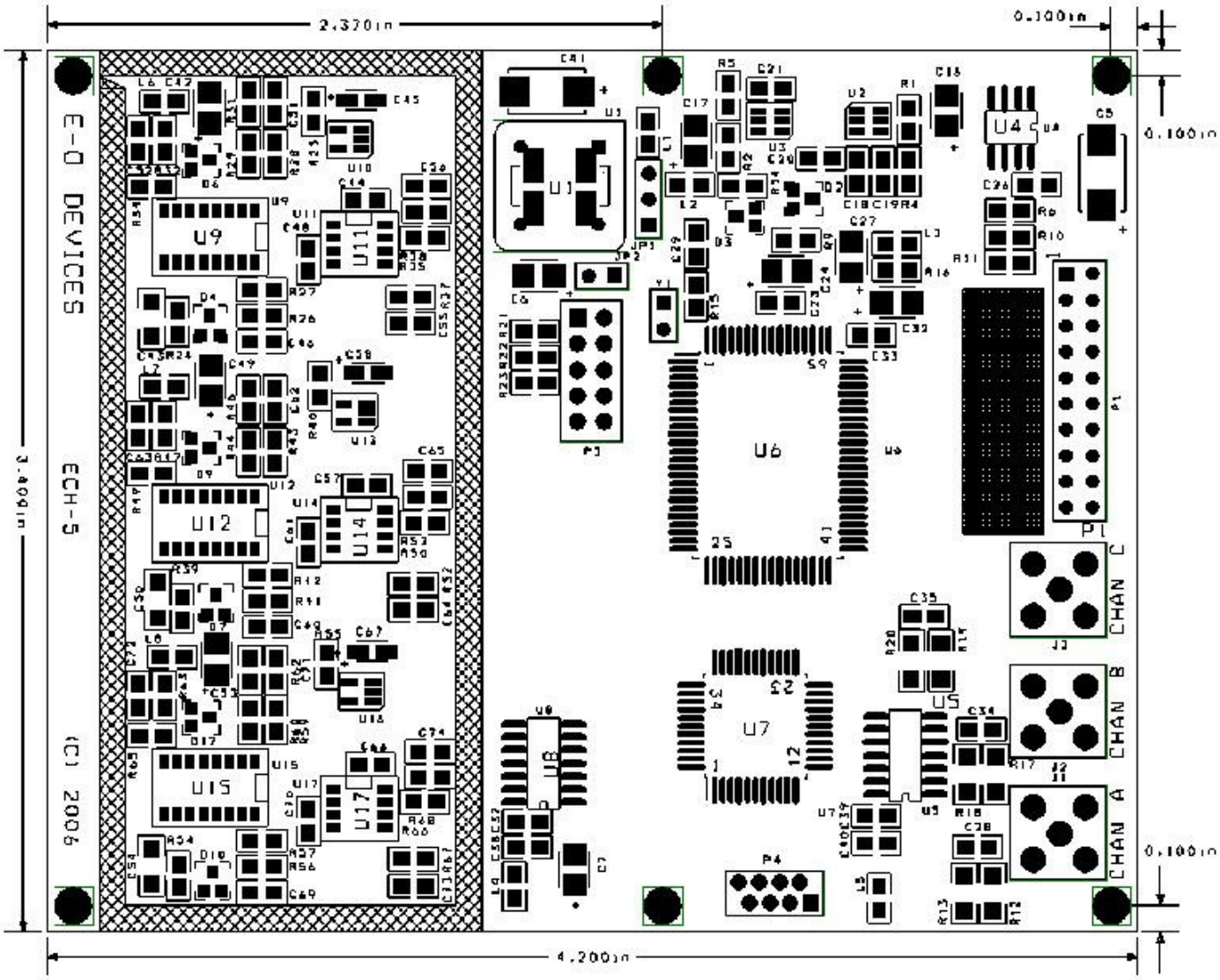
ORDERING CODES:

ECH – 5A	Standard chronometer
ECH – 5A – SMA	Standard chronometer with SMA timing connections
ECH – 5A – SMB	Standard chronometer with SMB timing connections
ECH – 5A – SMC	Standard chronometer with SMC timing connections

OPERATING SPECIFICATIONS: (-20C < Ta < +85C)

PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply Voltage[1]	4.85	5.0	5.15	Vdc
Supply Current[2]		250		mA
$t_{interval}$(IN), time interval range of measurement[3]	0.002		261.12	µs
$t_{resolution}$(IN), resolution of time interval measurement		15		ps
$t_{accuracy}$(IN), accuracy of time base		50		ppm
t_{error}, error of measurement (not including timebase accuracy) [4]		25	50	ps **(RMS)**
$t_{response}$, response time to data available after triggering[5]		30	40	µs

NOTES:
1. The external power supply must be regulated and filtered to +/- 0.15V.
2. During active measuring.
3. Adjustable by command from 1.28µs to 261.12µs in 1.28µs increments.
4. Standard time base accuracy is 50ppm.
5. Value at 1µs measurement. Time will increase proportionally with longer START-to-STOP times or range gates. Add 1µs for every 1µs longer START-to-STOP time or range gate (in case of a No-Return result).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E-O DEVICES
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